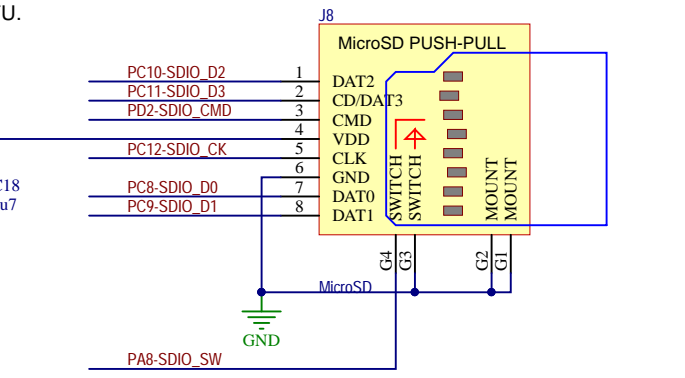
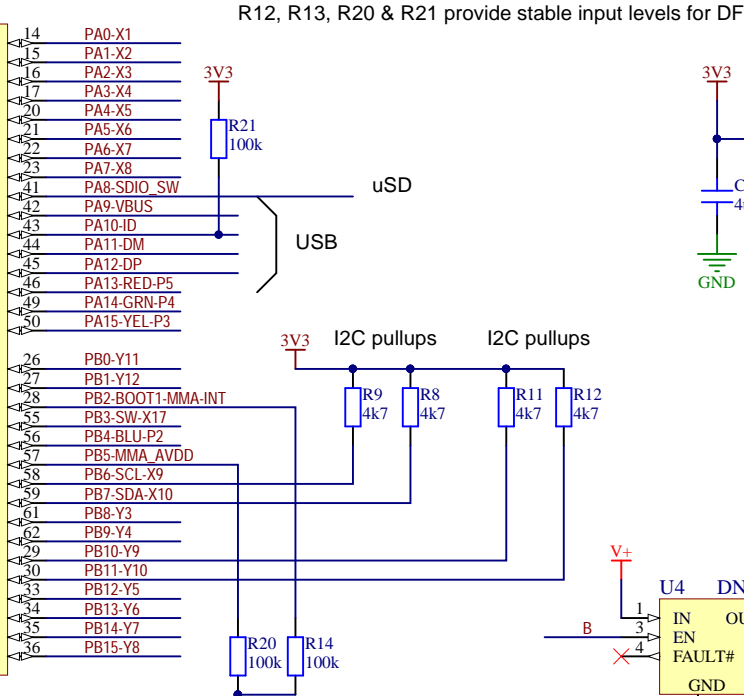
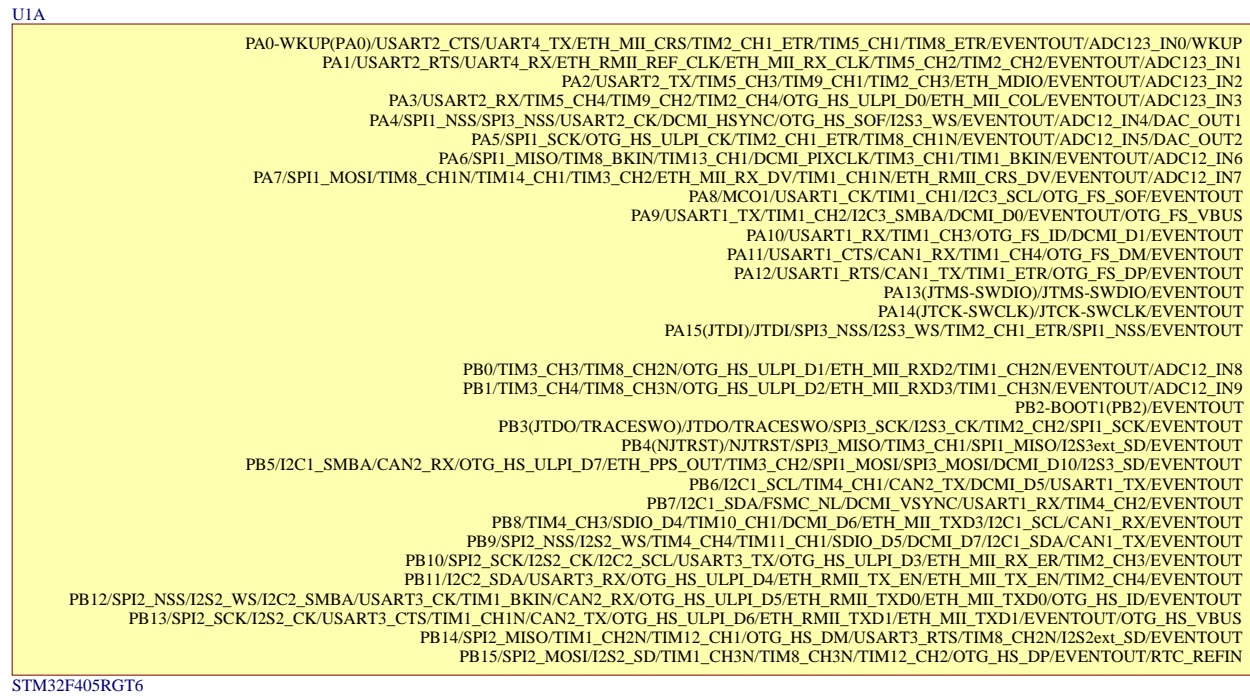
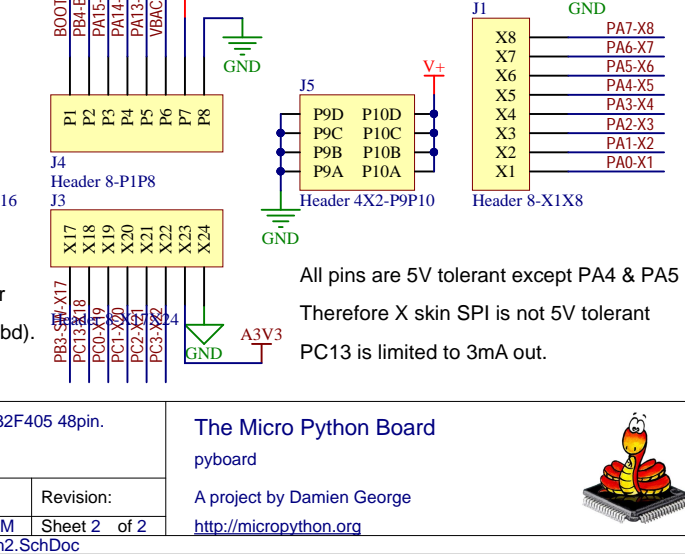
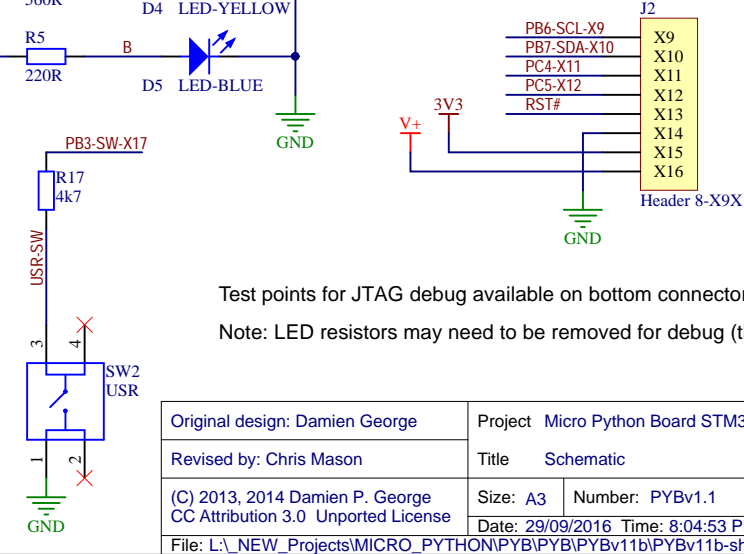
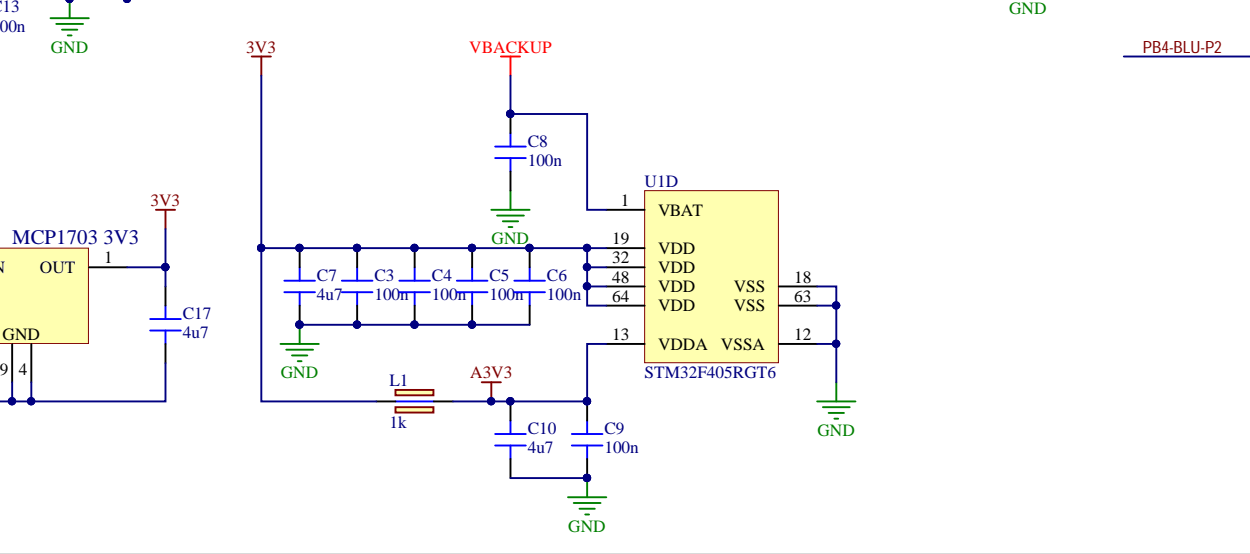
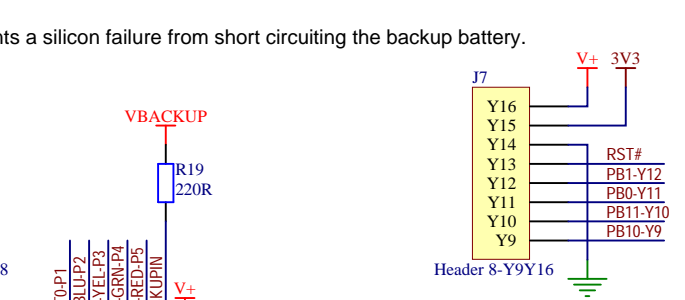
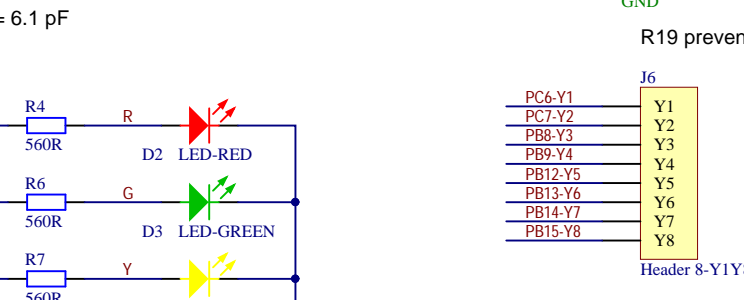
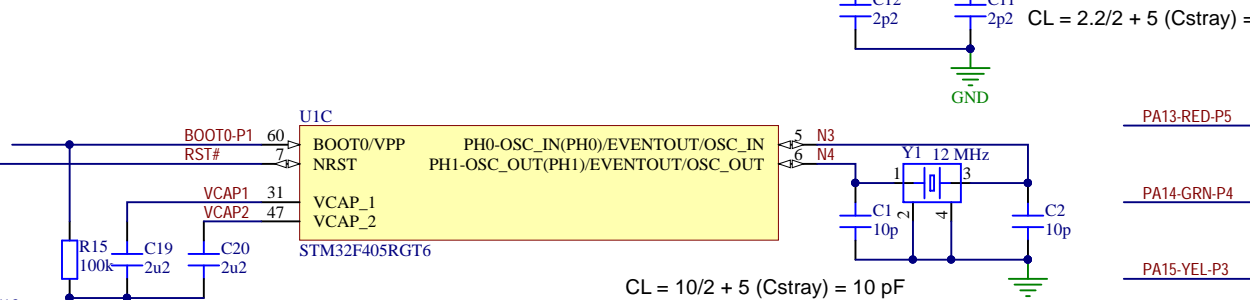
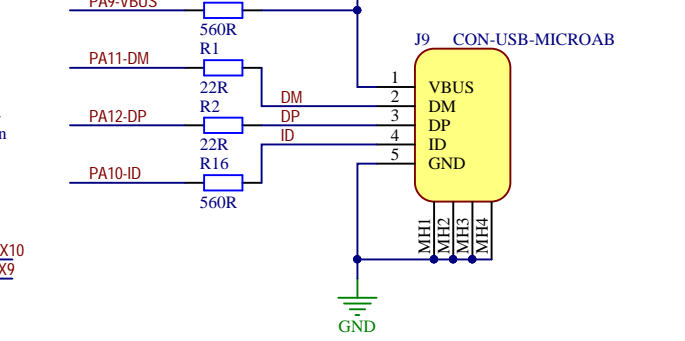
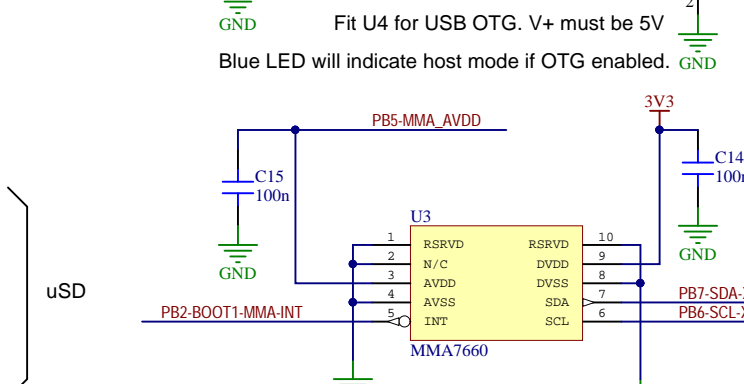
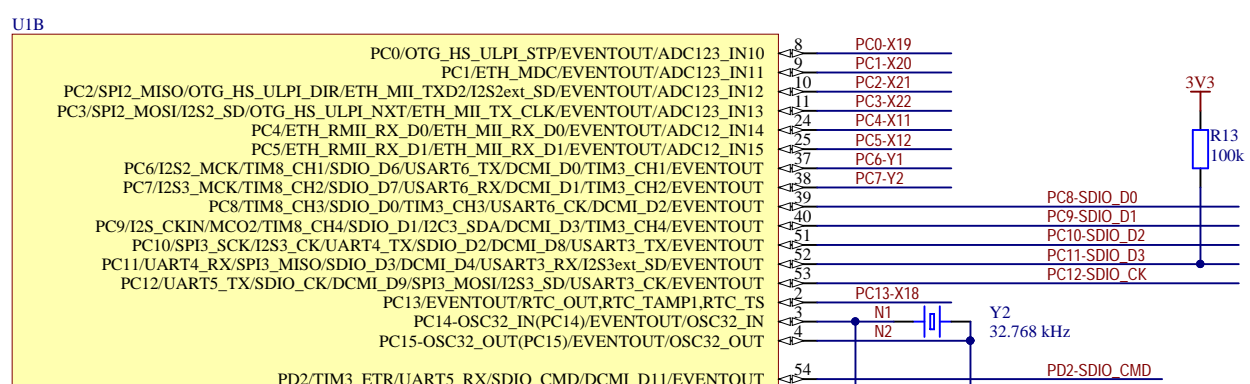
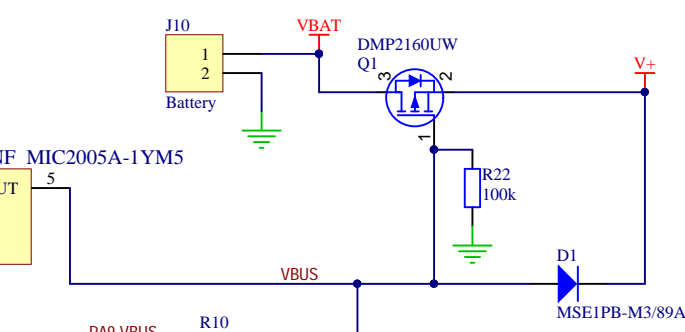


USB DFU requires stable levels on PA10, PB5, PB11 & PC11. PB2 must be low during boot.

R12, R13, R20 & R21 provide stable input levels for DFU.



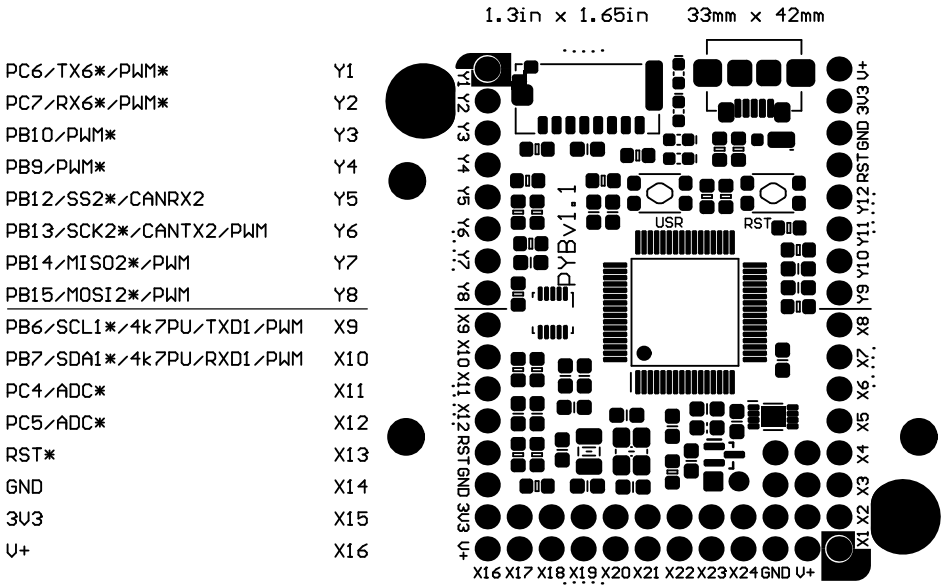
Q1 prevents VBUS (5V) from overcharging Lion / Lipo batteries.



Note: Functions marked * are standardised symmetrical functions.
 No serial port on Y9 & Y10. Use PYB for 4 serial ports.
 CANbus not available - use PYB.
 MCU: STM32F411.

Internal use ports

- PA9/OTG-VBUS
 - not supported/OTG-ID
 - PA11/USB-DM
 - PA12/USB-DP
-
- PC8/SDIO_DO
 - PC9/SDIO_D1
 - PC10/SDIO_D2
 - PC11/SDIO_D3
 - PC12/SDIO_CK
 - PA10/SDIO_SW
-
- PB6/SCL/MMA-SCL (shared with pin)
 - PB7/SDA/MMA-SDA (shared with pin)
 - PB2/BOOT1/MMA_INT
 - PB5/MMA_AVDD
-
- PB4/BLE_LED/JTAG-TRST (shared with pin)
 - PA13/RED_LED/JTAG-TMS/SWDIO (shared with pin)
 - PA14/GRN_LED/TCK/SWCLK (shared with pin)
 - PA15/YEL_LED/TDI (shared with pin)
 - PB3/USR_SW/TDO/TRACESW0 (shared with pin)

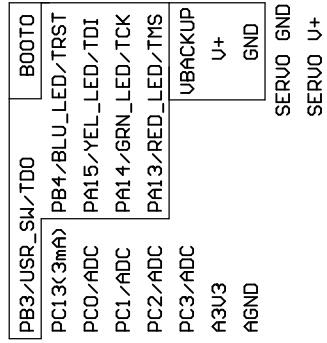


- PC6/TX6*/PWM* Y1
- PC7/RX6*/PWM* Y2
- PB10/PWM* Y3
- PB9/PWM* Y4
- PB12/SS2*/CANRX2 Y5
- PB13/SCK2*/CANTX2/PWM Y6
- PB14/MISO2*/PWM Y7
- PB15/MOSI2*/PWM Y8
- PB6/SCL1*/4k7PU/TXD1/PWM X9
- PB7/SDA1*/4k7PU/RXD1/PWM X10
- PC4/ADC* X11
- PC5/ADC* X12
- RST* X13
- GND X14
- 3V3 X15
- U+ X16

- Y16 U+
- Y15 3V3
- Y14 GND
- Y13 RST*
- Y12 PB1/ADC*/PWM
- Y11 PB0/ADC*/PWM
- Y10 PB8/SDA3*/4k7PU/PWM
- Y9 PA8/SCL3*/4k7PU/PWM
- X8 PA7/MOSI1*/ADC/PWM
- X7 PA6/MISO1*/ADC/PWM
- X6 PA5/SCK1*/ADC/DAC/PWM (3V3)
- X5 PA4/SS1*/ADC/DAC (3V3)
- X4 PA1/ADC/PWM*/SERVO
- X3 PA0/ADC/PWM*/SERVO
- X2 PA3/RX2*/ADC/PWM*/SERVO
- X1 PA2/TX2*/ADC/PWM*/SERVO

- X17 P1
- X18 P2
- X19 P3
- X20 P4
- X21 P5
- X22 P6
- X23 P7
- X24 P8
- PSA-D
- P10A-D

INNER ROW (P)



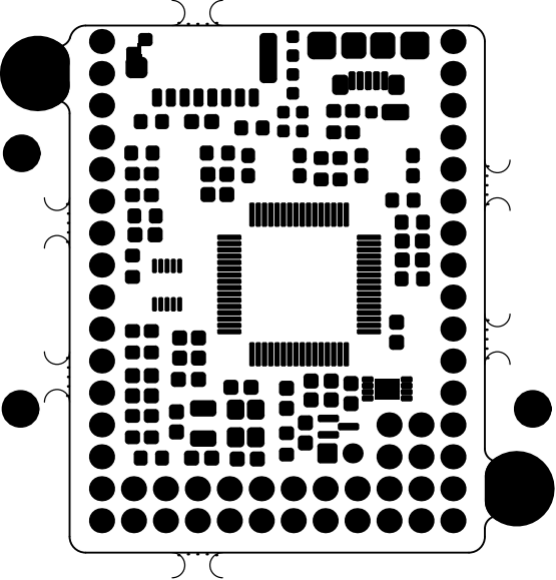
OUTER ROW (X)

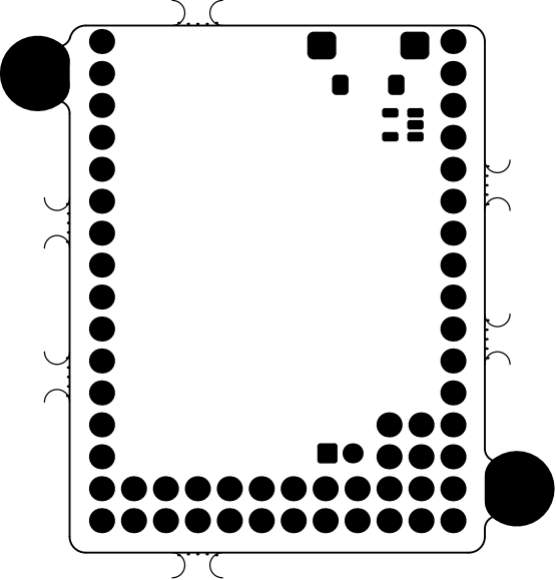
DESIGN RULES.

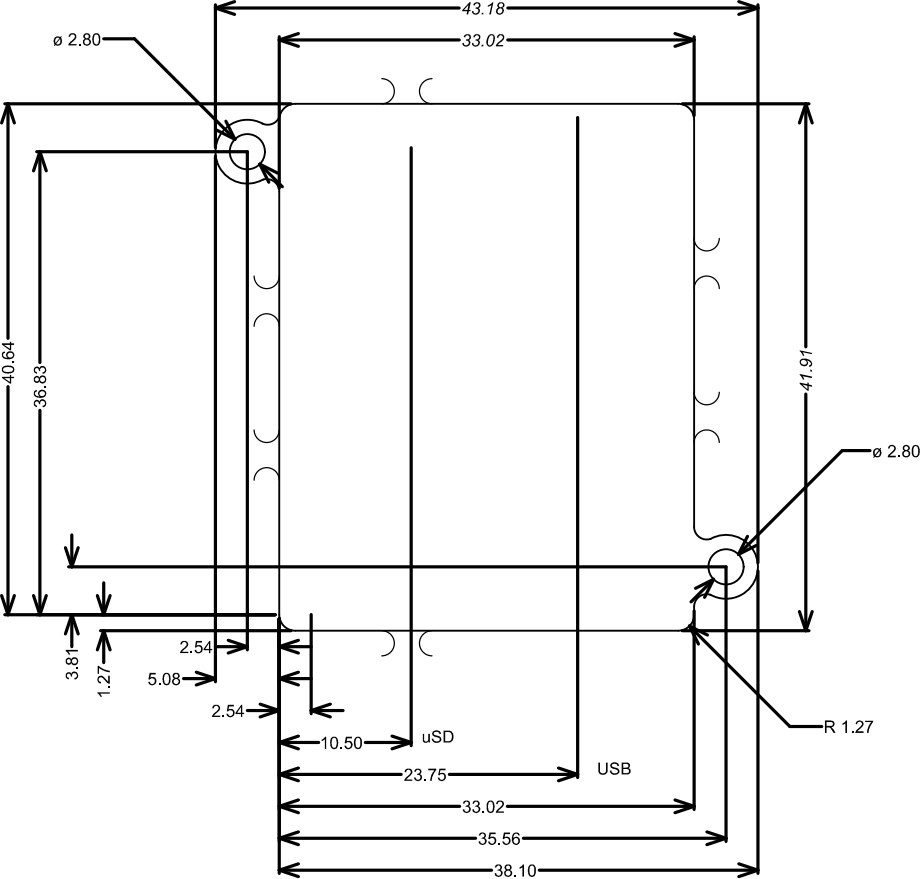
- Board profile and connector grid. 1.27mm (50mil).
- Component placement grid. 0.25mm
- Routing grid. 0.05mm
- Minimum track and spacing. 0.15mm (6mil).
- Minimum via size. Hole 0.25mm, pad 0.6mm.

PCB spec.

2 layer 1.6mm FR4. Green mask. White legend - 2 sides. Gold finish pb free. Electrical te







The board origin (0,0) is the bottom left corner of a half size skin compatible with X or Y position.
 The pyboard extends 1.27mm (50mil) below the origin to allow for labels on the bottom connector.
Dimensions in italics are for reference only.

U4

DNF MIC2005A-1YM5

J10



Battery

